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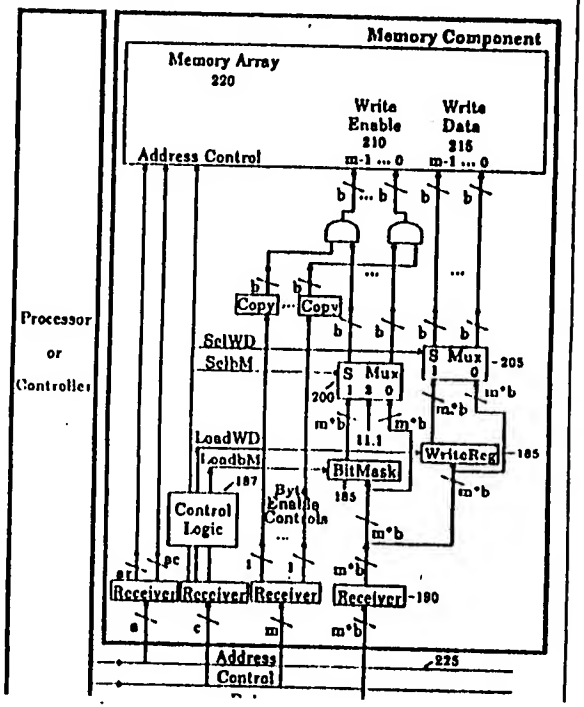
(54) Title: METHOD AND APPARATUS FOR WRITING TO MEMORY COMPONENTS

(57) Abstract

In the memory system of the present invention, additional operating modes are provided to enhance the functionality and performance of the memory system. In one embodiment, a unique bit mask is supplied with the write data used in each column access. In an alternate embodiment, a bit mask register and byte mask register are provided to support bit level and byte level masking. The bit mask and write data registers are realized as a single register to provide the functionality while minimizing component space and cost. In another embodiment, a separate bit mask and byte mask are provided. The byte mask is loaded with mask data in one cycle and is used during the next "q" column write accesses. This structure provides for operating modes with no bit masking, with bit masks supplied for every row access, and with bit masks supplied with every column access. In order to enhance the functionality of a system, such as a two-dimensional graphics system, in an alternate embodiment, the memory system is provided with two registers and a select control line to select data from one of two registers. In a computer graphics system, this is used to select between foreground and background colors. The embodiment can be utilized in conjunction with the other embodiments described to provide enhanced functionality and performance.



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METHOD AND APPARATUS FOR WRITING TO MEMORY COMPONENTS

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION:

The present invention relates to the control of data to be written to memory components. More particularly, the present invention relates to a structure and method for implementing bit and byte enable signals and logic during write operations to memory components.

2. ART BACKGROUND:

Figure 1 shows some of the common features of modern solid-state memory components. The memory components contain a two dimensional array of storage cells. These storage cells may be static (i.e. there is a bistable latch) or dynamic (i.e. there is a single capacitor holding a charge). A row of storage cells is read when a row address is applied to the row decoder and the appropriate read control signals are asserted. This entire row is held in a row of column amplifiers (sense amplifiers) which are typically static in nature. Any subset of this sensed row may be accessed via column addresses and control signals.

A write operation requires additional control. It is important to be able to write to a subset of a row. This is typically done as a two step process (although in a static memory component it may be done as a single step). The information to be written is placed on the write data signal lines. The write enable signal is asserted for only those bits of a row which has been selected by the column select circuitry and which are to be modified. Write enable signals are not asserted for the remaining bits. The Read/Write Column signal is then asserted, permitting those sense amplifiers of the row with the write enable signal asserted to be modified with the write data received across the write data signal lines. Subsequently, using the write row signals, the entire row may be rewritten from the column amplifiers back to the RAM array, with the subset of the storage cells modified according to the modified bits in the column amplifiers.

This technique works because the sense amplifier retains previous data written to the sense amplifier if the two write drivers driven by the write enable are allowed to float (write enable is not asserted). Although internally there is typically a write enable signal for each bit of write data, these signals are not available externally; therefore, most memory components are incapable of modifying any pattern of bits within a row.

Figure 3 shows an example of a prior art memory component with byte enable controls for write masking. Figure 3, and succeeding figures, use the notation set forth in Figure 2.

In the prior art memory components, the value of m is typically one or two. The memory array 110 and the data receiver 115 typically transact the same quantum of information (m*b bits). There are typically "m" write enable signals for masking the individual bytes of write data within this transaction quantum, where m represents the number of bytes of data communicated by the memory component. The masking is controlled by the byte enable controls 120. The copy block duplicates the bit on the one input wire onto the "b" output wires.

Figures 4 and 5 illustrate another example of prior art in which the memory component includes a bit enable register (BitMask) 180 and write data register (WriteReg) 185. In addition to the byte enable control lines shown in the previous example of Figure 3, two loadable internal registers, BitMask 180 and WriteReg 185 are connected to the receiver 190 for the data lines 195. Two multiplexers 200, 205 are provided for selecting the receiver 190 contents (the receivers typically have register or latch storage elements) or the contents of the two loadable registers 180, 185 for input to the write enable 210 and write data 215 input pins of the memory array 220.

As set forth in Figure 4, this configuration permits several modes of operation. The first mode provides the functionality of the previous example set forth in Figure 3. The second and sixth modes provide additional functionality.

Figure 6 illustrates a simplified timing diagram for the second mode. It should be noted that the signals for the row and column portions of the address are multiplexed together. In a typical operation, a row address is received and latched by the memory component, and followed by multiple column addresses in subsequent clock cycles to access the sensed row. Referring to Figures 5 and 6, when the row address Row[a] is received on the address lines 225, the BitMask[a] value is also received on the data lines 195. The BitMask[a] value is latched by the bit mask register 180, and is used to perform bit masking on incoming data until a new value is received to overwrite it.

When each column address Col[a,i] is received on the address lines 225, the WData[a,i] value is also received on the data lines 195. This value is held in the receiver 190, and is used to drive the write data inputs 215 of the memory array 220. This is repeated for "n" different values of WData, using the same value of BitMask stored in the bit mask register 180. When the next row address Row[b] is received on the Address lines 225, a new BitMask[b] value is also

received on the data lines 195. A second series of column write operations is then performed with the new bit mask value.

Figure 7 shows a simplified timing diagram for Mode Six. Referring to Figures 6 and 7, then the row address Row[a] is received on the address lines 225, the WData[a] value is also received on the data lines 195. This value is latched by the WriteReg register 185, and is used until a new WData[a] value is received and overwrites the value in the register 185. Thus, when each column address Col[a,i] is received on the address lines 225, the BitMask[a,i] value is also received on the data lines 195. This value is held in the receiver 190, and subsequently drives the Write enable inputs 210 of the Memory Array 220. This is repeated for "n" different values of the bit mask, using the same value stored in the WriteReg 185.

When the next row address Row[b] is received on the address lines 225, a new WData[b] value is also received on the data lines 195. A second series of column writes operations is then performed using the new WData[b] value.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a sophisticated level of bit and byte masking in a memory system.

It is an object of the present invention to provide a memory system which can receive a new bit mask with each "m*b" bits of write data sent to the memory array.

In the memory system of the present invention, additional operating modes are provided to enhance the functionality and performance of the memory system. In one embodiment, a unique bit mask is supplied with the write data used in each column access. In an alternate embodiment, a bit mask register and byte mask register are provided to support bit level and byte level masking. Alternatively, the bit mask and write data Register are realized as a single register to provide the same functionality. These two registers are realized as a single register to provide the functionality while minimizing component space and cost.

In another embodiment, a separate bit mask and byte mask are provided. The byte mask is loaded with mask data in one cycle and is used during the next "b" column write accesses. This structure provides for operating modes with no bit masking, with bit

masks supplied for every row access and with bit masks supplied with every column access.

In order to enhance the functionality of a system, such as a two-dimensional graphics system, in an alternate embodiment, the memory system is provided with two registers and a select control line to select data from one of two registers. In a computer graphics system, this is used to select between foreground and background colors. The embodiment can be utilized in conjunction with the other embodiments described to provide enhanced functionality and performance.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features and advantages of the present invention will be apparent from the following detailed description in which:

Figure 1 is a block diagram illustration of the internal structure of a memory component.

Figure 2 is a table which sets forth the notation for the block diagrams shown.

Figure 3 is a block diagram illustration of a prior art memory system with byte enable control.

Figure 4 is a table illustrating the possible operating modes in the prior art memory system of Figure 3.

Figure 5 is a block diagram illustration of a prior art memory system with a bit enable register.

Figures 6 and 7 are illustrations of the timing for two modes of the prior art memory system of Figure 5.

Figure 8 is a block diagram illustration of one embodiment of the memory system of the present invention.

Figures 9a and 9b illustrate the timing for two modes of the memory system of the present invention.

Figure 10 is a block diagram illustration of one embodiment of the memory system of the present invention.

Figure 11 is a block diagram illustration of an alternate embodiment of the memory system of the present invention.

Figure 12 illustrates the timing for one mode of the memory system of the present invention illustrated in Figure 11.

Figure 13 is a block diagram illustration of an alternate embodiment of the memory system of the present invention.

Figure 14 illustrates the timing for one mode of the embodiment shown in Figure 13.

Figure 15 is a table summarizing the operating modes available for the different embodiments of the memory system of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following description, for purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details are not required in order to practice the present invention. In other instances, well known electrical circuits and structures are shown in block diagram form in order not to obscure the present invention unnecessarily.

Figure 8 is a block diagram of one embodiment. The data paths are similar to those shown in Figure 5. However, control logic 187, provides the control signals necessary. For the data and bit mask transfer as shown by the timing diagrams of Figures 9a and 9b.

Figures 9a and 9b respectively illustrate the timing for two new modes hereinafter referred to as modes seven and eight, in accordance with the teachings of the present invention.

Referring to Figure 9a , the row address Row[a] is received on the address lines. Prior to the issuance of each column address Col[a,i], a BitMask[a,i] value is received and latched into the BitMask register. When each column address Col[a,i] is received on the address lines, the WData[a,i] value is also received on the Data wires. This WData[a,i] value is held in the receiver, and is subsequently used

to drive the write data inputs to the memory array. This two cycle sequence is repeated for "n" different pairs of BitMask and WData values. Each column address can be received during the mask data cycle to provide more time to perform the access.

Mode seven, as illustrated in Figure 9a, provides a significant performance advantage over, for example, mode two for the situation when a different bit mask must be applied to each piece of data to be written (WriteData) during a write operation. Mode seven of the system of the present invention is able to perform a write operation to the memory array in every two clock cycles of the interface, whereas mode two requires a new row access operation to apply a different bit mask to each piece of WriteData. As is well known in the art, a new row access typically takes four to eight times as long as a column access.

Figure 9b illustrates the timing for Mode eight. The row address Row[a], and column addresses Col[a,1] - Col[a,n] are received on the address lines. Prior to receipt of each column address Col[a,i], a WData[ai] value is received on the data lines and latched into the WriteReg register. When each column address Col[a,i] is received on the address lines, the BitMask[a,i] value is also received on the data lines. This value is held in the receiver, and drives the write enable inputs of the memory array. This two cycle sequence is repeated for "n" different pairs of WData and BitMask. The column address can be

received when the write data is received, thereby providing more time to perform the access.

Mode eight is thus very similar to mode seven, with the only difference being the order in which BitMask and WData are supplied in each column write cycle. Thus, the same performance advantages are realized.

There are several trends in memory component design which will affect the techniques used for write control. These trends include the increase of interface speed (receivers and transmitters) relative to the speed of the memory array, and the multiplexing of control information onto data lines.

Figure 10 illustrates a memory array and interface circuit. Referring to Figure 10, the impact of increasing interface speed on a memory component can be shown. The number of data lines (d) 300 is less than the number of write data and write enable lines 305, 310 (m*b). The ratio of m*b/d is the same as the ratio of the cycle time of the memory array compared to the bit transmission across a time of a data line. With an aggressive interface technology this ratio might be eight or greater.

The greater the ratio, the larger the size of the BitMask and WriteReg registers. One optimization is to combine the two registers

into a single BitMask register 320. At any time, this register holds either the bit mask or write data. Any drawbacks incurred for combining the registers is far outweighed by the space savings and cost savings enjoyed by eliminating a register.

As more information is written during each memory array cycle, it is also important to provide enough byte enable controls. This may be done, as before, by using "m" 325 control lines as dedicated byte enable control signals. This permits the most flexible control for applications requiring the manipulation of byte-sized quantities of information.

However, some memory components may not be able to dedicate "m" control lines for this control function. Instead, referring to Figure 11, the byte mask control signals are multiplexed on the data lines 300 (like the bit mask controls). A byte mask register 380, is provided which enables a static set of byte enable signals to be loaded and used on multiple sets of write data during write operations by controlling the load byte mask (LoadBM) and select byte mask (SelBM) signals. Alternatively, a byte mask of m*q bits may be loaded into the byte mask register 380 prior to receiving each "q" (where q can be typically equal to b or b-1, depending upon implementation) blocks of m*b write data bits, since each byte mask bit controls "b" write data bits. It should be noted that, in the present embodiment, a multiplexer 390 with "q+1" inputs of "m" bits each is needed in order

to select the proper byte mask for each block of data (and to also provide for selectively bypassing the byte mask and forcing all ones). It should be apparent that one can generate byte enable signals utilizing a compact encoding such as providing only the starting address and length information. Compact encoding technique can be applied to all embodiments. It should also be apparent that by storing values in both the bit mask and write data registers, and using those values multiple times with different addresses (under control of internal control logic), large bandwidth savings are permitted.

Figure 12 illustrates the timing of a write operation in accordance with operating mode twenty one using the byte mask register as illustrated in the embodiment of Figure 11. This operating mode can be viewed as an extension of operating mode one, wherein an additional clock cycle is used to transmit the byte mask. A row address is received in the first clock cycle. In the next cycle an "m*b" bit value ByteMask[a] is loaded into the byte mask register. In the next "q" column write accesses, a value WData[a,i] is received and driven to the write data inputs of the Memory Array. In each write access, one of the "b" values (each of which are "m" bits wide) is selected from the byte mask register and applied to the write enable inputs of the memory array.

Although a clock cycle is added to load the byte mask register, reducing the data bandwidth by 1/b, "m" byte enable control pins have

been saved. In addition, the controller is relieved of the burden of merging the bit and byte masks. In a similar manner, operating modes two, six, seven, and eight can be extended to add a cycle to load the ByteMask register with a byte mask prior to every "b" column write accesses, thereby providing new operating modes modes 22 through 28.

In two-dimensional graphics systems it is advantageous to be able to write one of two color values into each pixel under control of a select mask. The two color values represent a foreground and a background color. The select mask chooses one of the two colors.

Figure 13 illustrates an embodiment of the memory system of the present invention which provides this capability. The multiplexer 500 receives "m*b" bits from the WRegF 505 and WRegB 510 registers, and gets "m*b" select bits from the data receiver 515. Figure 14 illustrates the timing of the memory system of the prevent invention operating in mode one using with the two registers 505, 510. Referring to Figures 13 and 14, a row address is received by receiver 520 in the first cycle. In the next cycle an "m*b" bit value foreground color is loaded into the WRegF register 505. In the following cycle an "m*b" bit value background color is loaded into the WRegF register 510. In the next "n" column write accesses, a value WSel[a,i] is received and selects between the two color values on a bit-by-bit basis. Although no bitmask or bytemask is used in the above

example, as shown in Figure 13, the system is extendable to handle the additional functionality.

In a similar manner, operating modes two through eight can also be extended to include the two color registers and select signals, resulting in new modes 102 through 108.

Figure 15 summarizes all the writing mode combinations that have been discussed, as well as all other combinations that have been implied. The first eight modes include the prior art writing modes and new extensions described earlier. Modes 11-18 are similar to modes 1-8, except that the byte mask is supplied by a single internal register rather than control inputs, as shown in Figure 10. Likewise, in modes 21-28, the byte mask is supplied by the data input signal lines, interleaved with data input, as shown in Figure 12, for other functions.

Modes 101, 102, 107, and 108 are similar to modes 1, 2, 7, and 8 except that the write data is supplied by two internal color registers and select information from the data inputs (combinations 3, 4, 5, and 6 are not applicable since the write data is not dependent upon the data input in these cases). Likewise, modes 111 through 118 are similar to modes 11 through 18 with the difference in the source of the write data, and modes 121 through 128 are similar to modes 21

through 28. Modes 201 through 628 permute the WDataF, WDataB, and WSelect sources through all relevant combinations.

The invention has been described in conjunction with a preferred embodiment. It is evident that numerous alternatives, modifications, variations and uses will be apparent to those skilled in the art in light of the foregoing description.

CLAIMS

What is claimed is:

1. In a memory system comprising at least one memory coupled to a bus, a method for performing masking of bits during a write operation comprising the steps of:

(a) issuing a row address across the bus to the memory;

(b) said memory sensing said row identified by the row address;

(c) issuing a bit mask identifying those bits to be masked during a write operation;

(d) issuing write data to be written to the memory array;

performing steps (c) and (d) for each write data to be written to the memory array;

wherein the write data can be individually masked on a bit-by-bit basis.

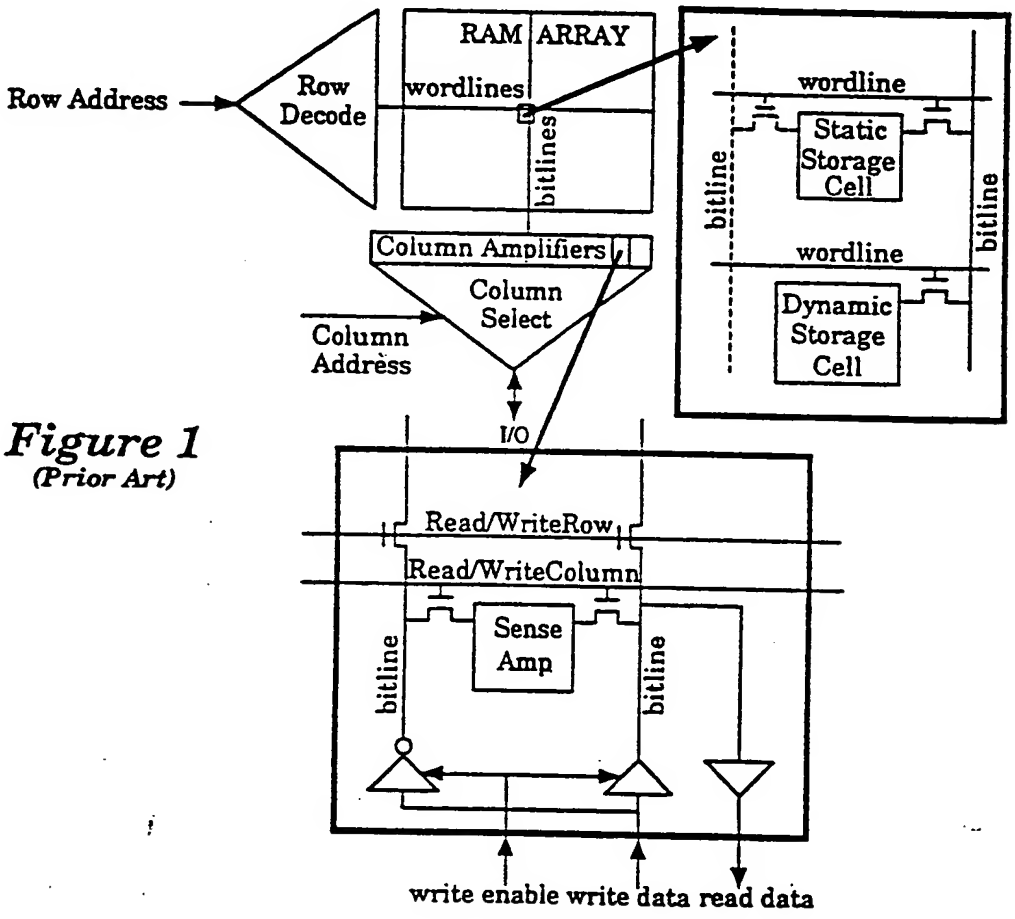


Figure 1
(Prior Art)

Term	Description
Address	The wires used to send the row and column addresses from the controller to the memory component.
Data	The wires used to send the write data from the controller to the memory component, or to return the read data to the controller.
Control	The wires used to send the control information from the controller to the memory component. This includes signals such as RAS (row address strobe), CAS (column address strobe), CS (chip select), and WE (write enable).
a	Number of external Address wires received by the memory component
ar	Number of row Address wires received by the memory component to perform an access
ac	Number of column Address wires received by the memory component to perform an access
c	Number of Control wires received by the memory component
b	The number of bits in a byte of information (typically eight or nine).
m	Number of bytes of Data wires received (or transmitted) by the memory component
WriteEnable	The wires used to send the writeenable information to the Sense Amps.
WriteData	The wires used to send the writedata information to the Sense Amps.

Figure 2
(Prior Art)

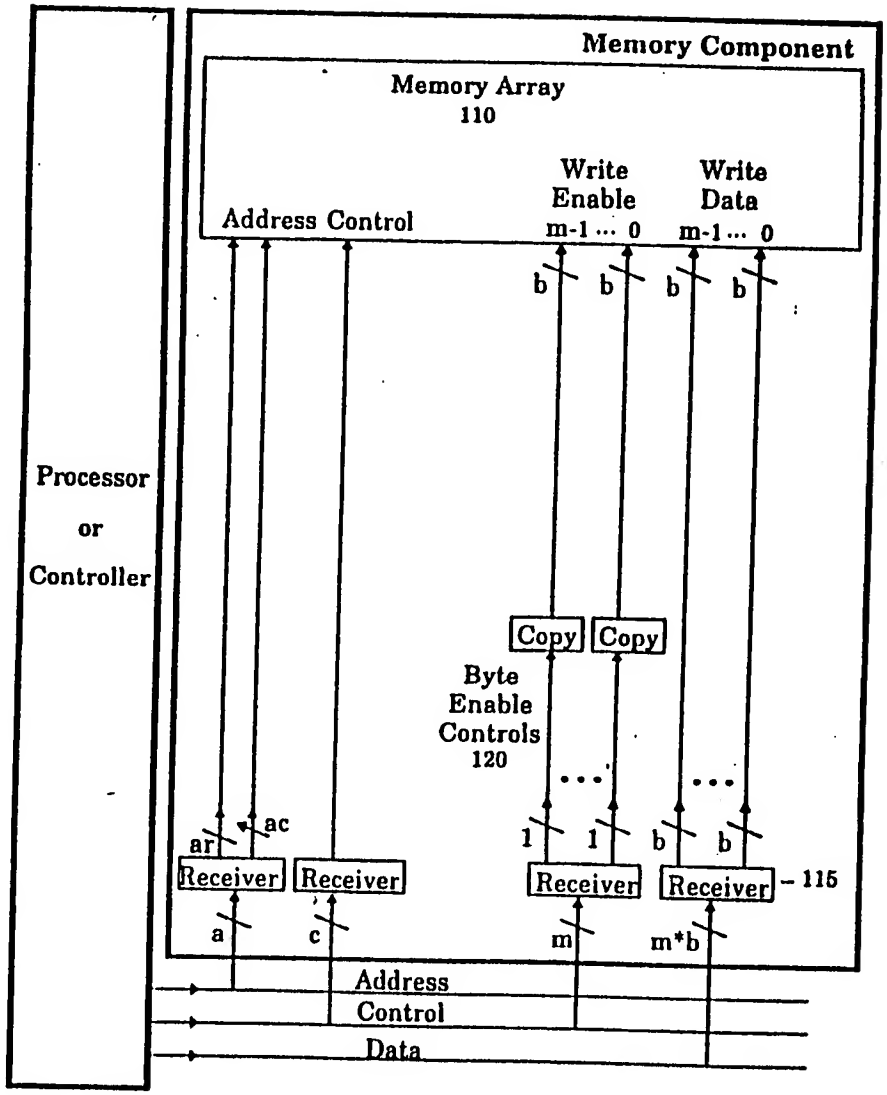


Figure 3
(Prior Art)

Number	Mode	Description
1	SelWD = 0 SelbM = 2 LoadWD not used LoadbM not used	This mode permits operation that is equivalent to the previous example; that is, the Receiver Data is placed onto the WriteData inputs of the Memory Array, and the WriteEnable inputs are controlled with the "m" Byte Enable controls.
2	SelWD = 0 SelbM = 1 LoadWD not used LoadbM = 1	This mode permits the BitMask register to loaded and then used repeatedly for different WriteData (held in the Data receivers) on successive column write operations.
6	SelWD = 1 SelbM = 0 LoadWD = 1 LoadbM = not used	This mode permits the WriteReg register to loaded and then used repeatedly with different BitMasks (held in the Data receivers) on successive column write operations.

Figure 4
(Prior Art)

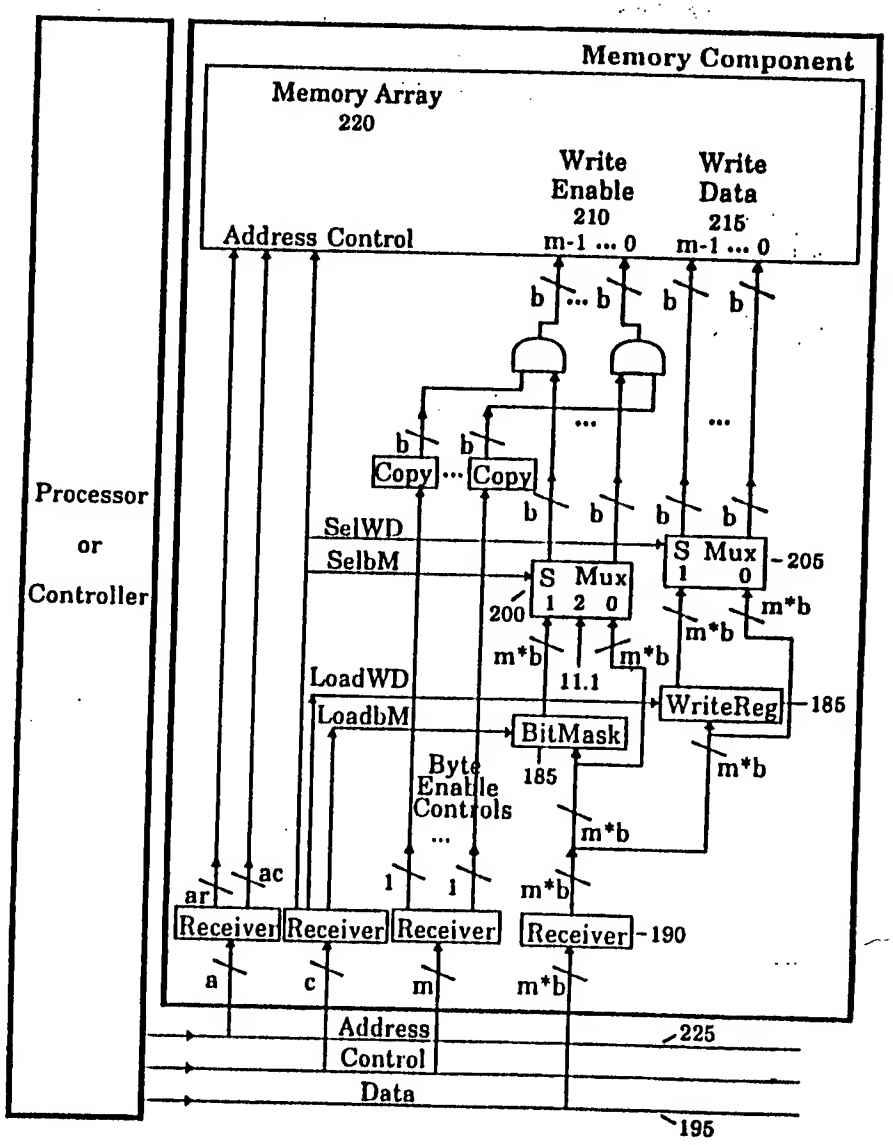


Figure 5
(Prior Art)

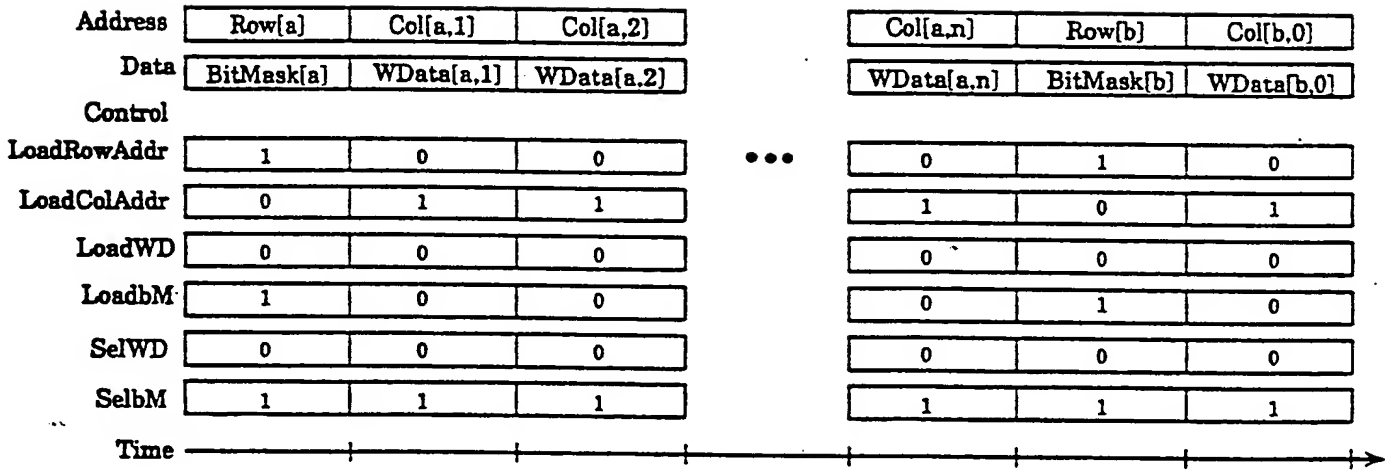


Figure 6
(Prior Art)

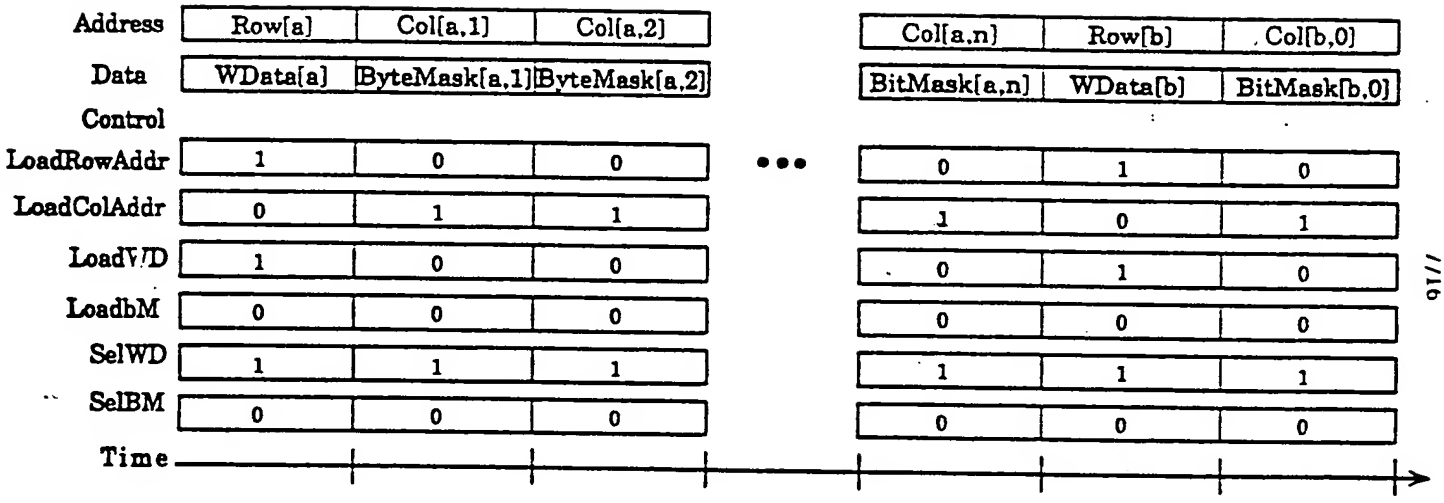
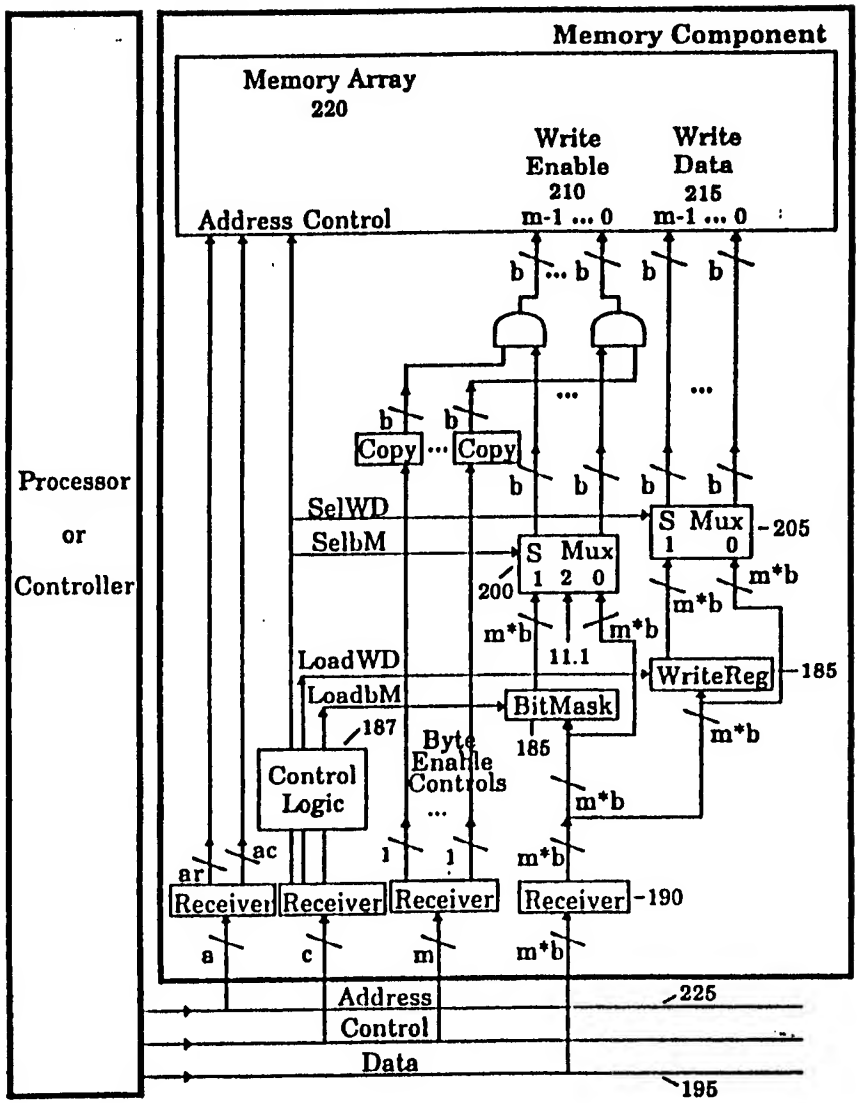


Figure 7
(Prior Art)


Memory Component
Memory Array
220
Write
Enable
210
Write
Data
215
Address Control
m-1 ... 0
m-1 ... 0
Processor
or
Controller
Copy
Copy
SelWD
SelbM
S Mux
1 0
205
S Mux
1 2 0
200
m*b
11.1
LoadWD
LoadbM
WriteReg
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BitMask
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Byte
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Controls
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Receiver
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a
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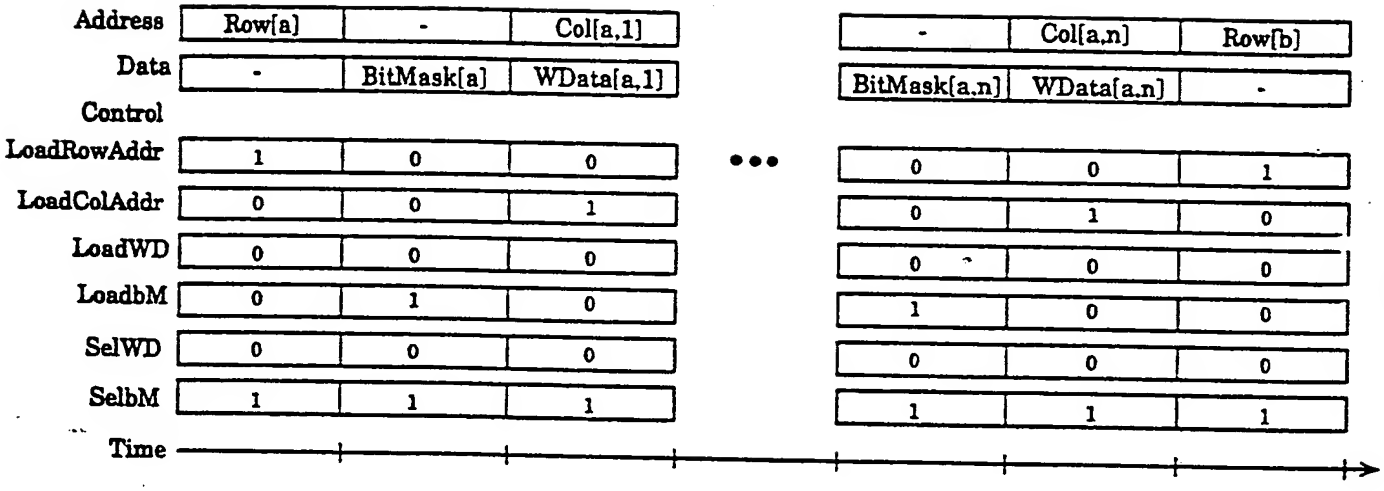
Address
Control
Data
225
195

Figure 8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SelbM
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-
Col[a,1]
-
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WData[a,1]
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0 0 1
0 0 0
0 1 0
0 0 0
1 1 1
-
Col[a,n]
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-
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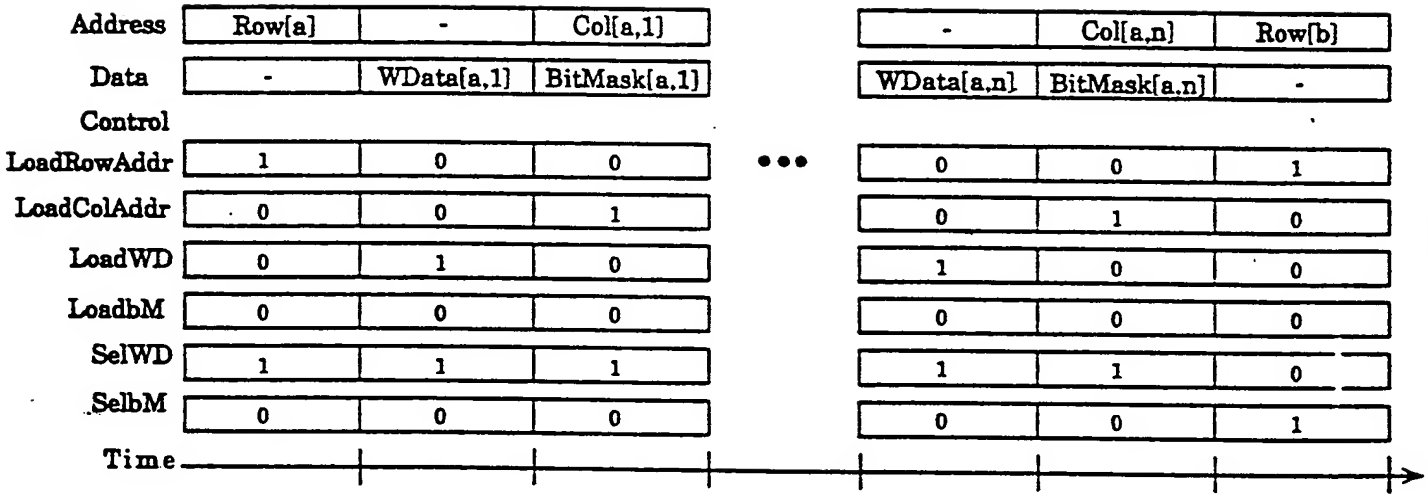
0 0 0
1 0 0
0 0 0
1 1 1

Figure 9a


Address
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Col[a,n]
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Data
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WData[a,1]
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BitMask[a,n]
-
Control
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LoadColAddr
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LoadWD
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LoadbM
0 0 0 0 0 0
SelWD
1 1 1 1 1 0
SelbM
0 0 0 0 0 1
Time

Figure 9b

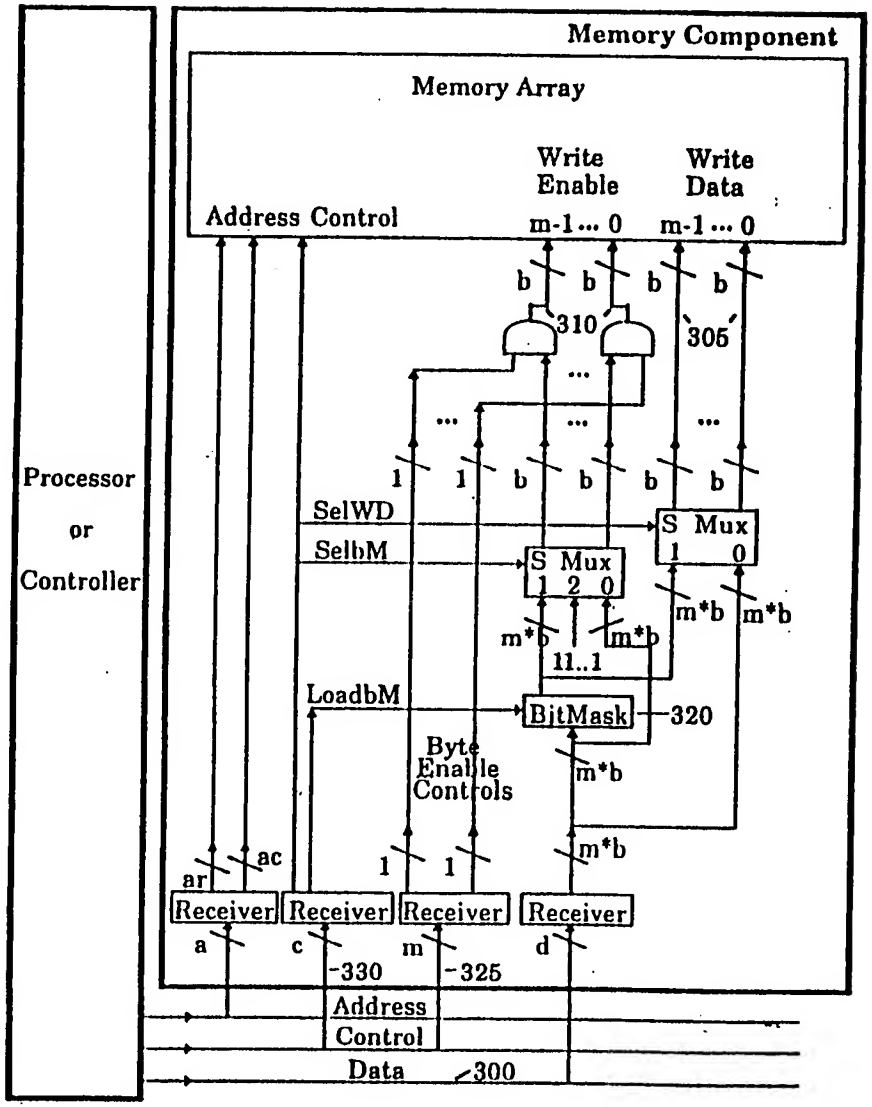
Memory Component
Memory Array
Write Enable
Write Data
Address Control
m-1 ... 0
m-1 ... 0
b
310
305
1
SelWD
SelbM
S Mux
1 0
S Mux
1 2 0
m*b
11..1
LoadbM
BitMask
320
Byte Enable Controls
ar
ac
Receiver
Receiver
Receiver
Receiver
a
c
m
d
330
325
Address Control
Data
300
Processor or Controller

Figure 10

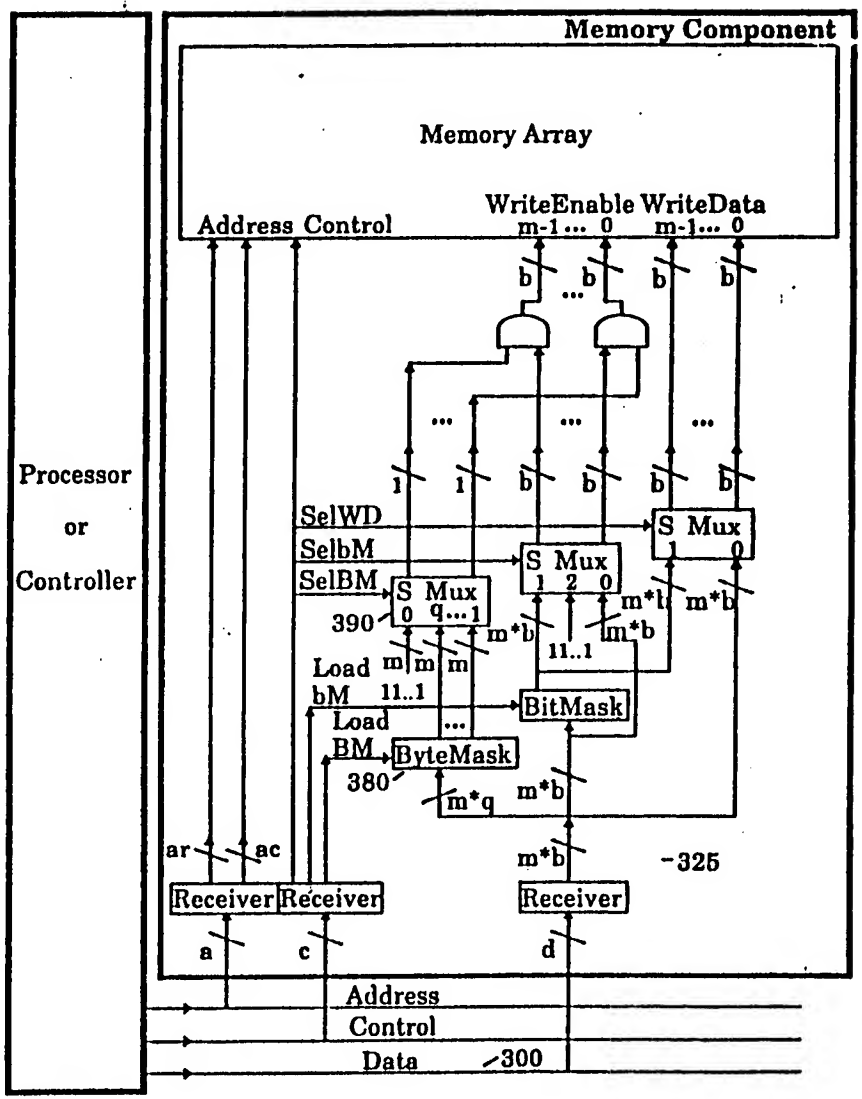
Memory Component
Memory Array
Address Control
WriteEnable WriteData
m-1 ... 0
m-1... 0
Processor
or
Controller
SelWD
SelbM
SelBM
S Mux
390
Load
bM
11..1
BitMask
Load
BM
ByteMask
380
m*q
m*b
ar
ac
-325
Receiver
Receiver
Receiver
a
c
d
Address
Control
Data
300

Figure 11

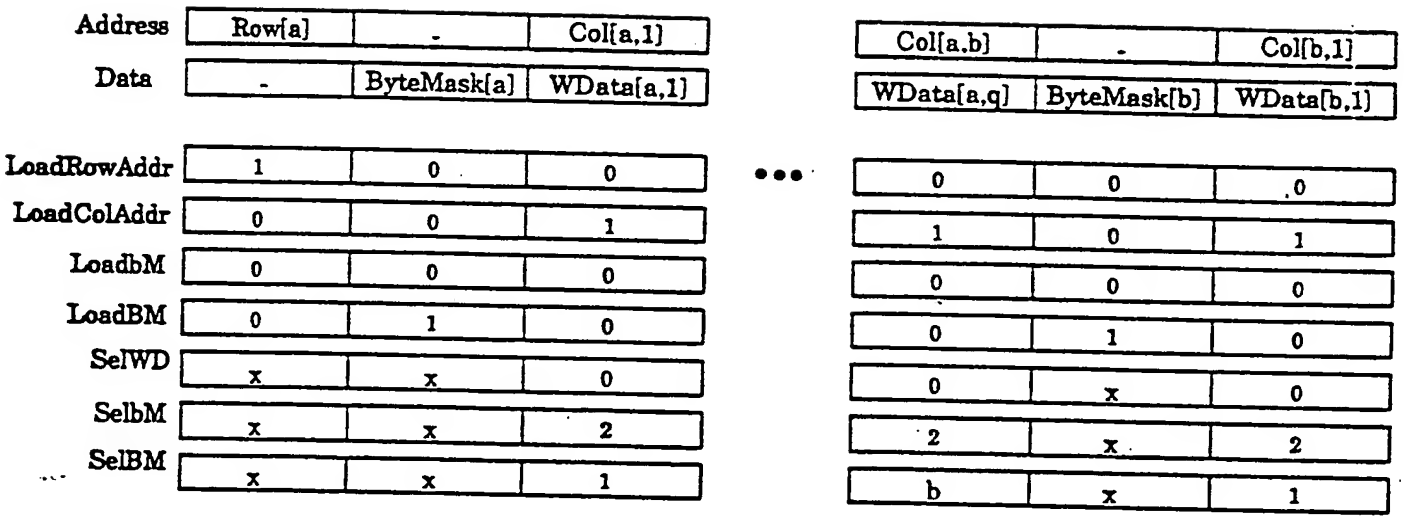
Address
Row[a]
-
Col[a,1]
Col[a,b]
-
Col[b,1]
Data
-
ByteMask[a]
WData[a,1]
WData[a,q]
ByteMask[b]
WData[b,1]
LoadRowAddr
LoadColAddr
LoadbM
LoadBM
SelWD
SelbM
SelBM
1 0 0
0 0 1
0 0 0
0 1 0
x x 0
x x 2
x x 1
0 0 0
1 0 1
0 0 0
0 1 0
0 x 0
2 x 2
b x 1

Figure 12

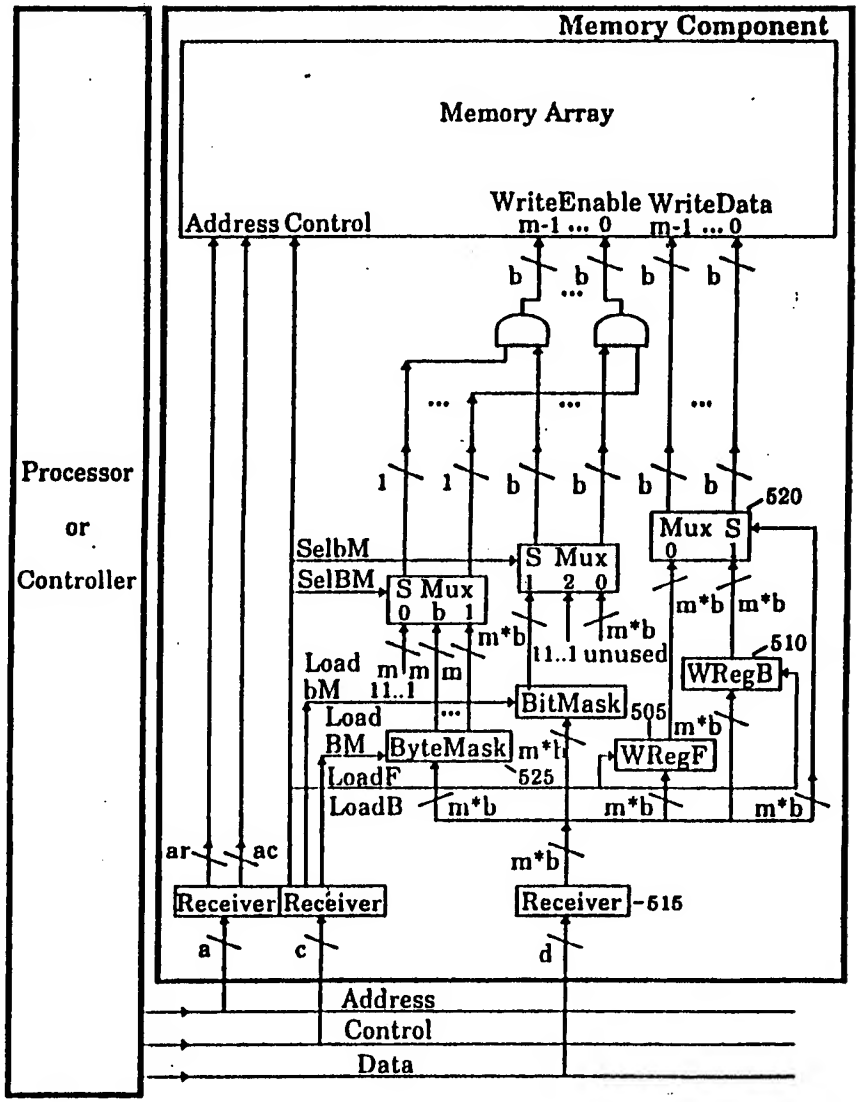
Memory Component
Memory Array
Address Control
WriteEnable m-1 ... 0
WriteData m-1 ... 0
Processor
or
Controller
SelbM
SelBM
S Mux
0 b 1
S Mux
1 2 0
Mux S
0 1
520
m*b
11..1 unused
510
WRegB
Load
bM 11..1
BitMask
505
Load
BM
ByteMask
WRegF
LoadF
525
LoadB
ar
ac
Receiver
Receiver
Receiver
515
a
c
d
Address
Control
Data

Figure 13

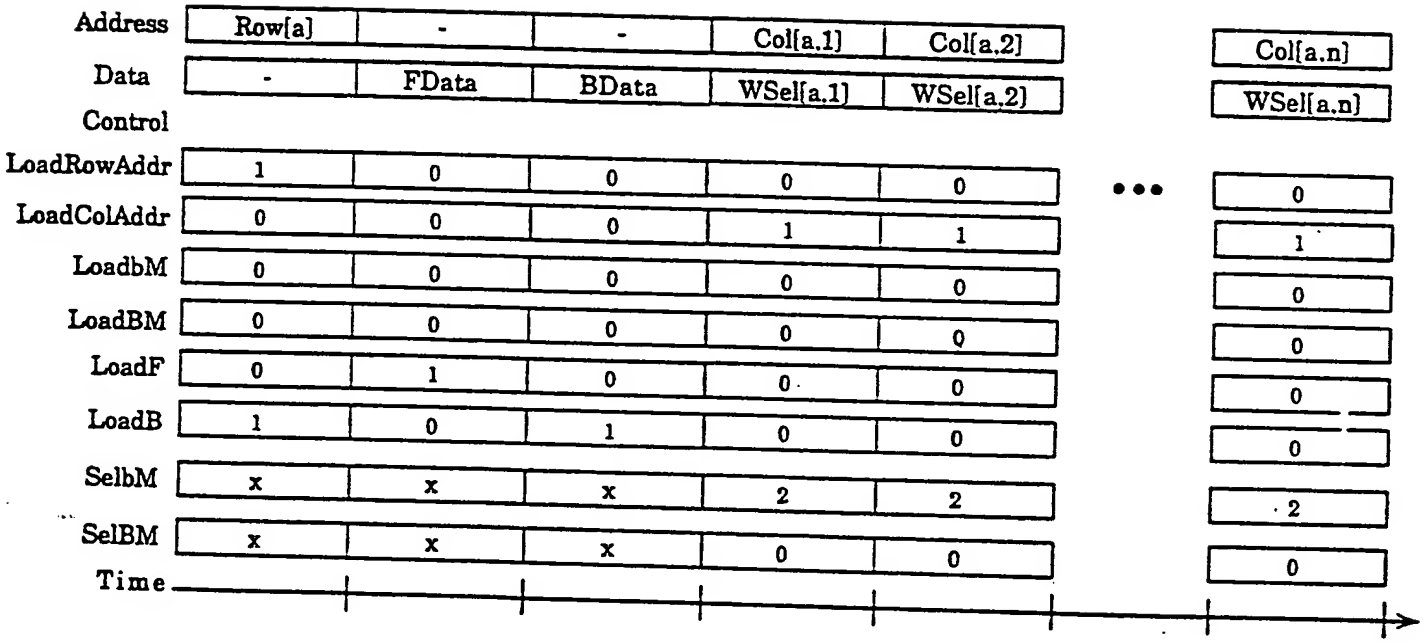
Address
Row[a]
-
-
Col[a,1]
Col[a,2]
Col[a,n]
Data
-
FData
BData
WSel[a,1]
WSel[a,2]
WSel[a,n]
Control
LoadRowAddr
1 0 0 0 0 0
LoadColAddr
0 0 0 1 1 1
LoadbM
0 0 0 0 0 0
LoadBM
0 0 0 0 0 0
LoadF
0 1 0 0 0 0
LoadB
1 0 1 0 0 0
SelbM
x x x 2 2 2
SelBM
x x x 0 0 0
Time

Figure 14

Number	ByteMask	BitMask	WDataF	WDataB	WSelect
1 (prior art)	Control Input	1..11	Data Input	Not Used	Not Used
2 (prior art)	Control Input	Register	Data Input	Not Used	Not Used
3	Control Input	Data Input	Data Input	Not Used	Not Used
4	Control Input	1..11	Register	Not Used	Not Used
5	Control Input	Register	Register	Not Used	Not Used
6 (prior art)	Control Input	Data Input	Register	Not Used	Not Used
7	Control Input	Data Input	Data Input	Not Used	Not Used
8	Control Input	Data Input	Data Input	Not Used	Not Used
11 -18	Register	as above	as above	Not Used	Not Used
21 -28	Data Input	as above	as above	Not Used	Not Used
101	Control Input	1..11	Register	Register	Data Input
102	Control Input	Register	Register	Register	Data Input
107	Control Input	Data Input	Register	Register	Data Input
108	Control Input	Data Input	Register	Register	Data Input
111	Register	1..11	Register	Register	Data Input
112	Register	Register	Register	Register	Data Input
117	Register	Data Input	Register	Register	Data Input
118	Register	Data Input	Register	Register	Data Input
121	Data Input	1..11	Register	Register	Data Input
122	Data Input	Register	Register	Register	Data Input
127	Data Input	Data Input	Register	Register	Data Input
128	Data Input	Data Input	Register	Register	Data Input
201 - 228	as above	as above	Register	Data Input	Register
301 - 328	as above	as above	Data Input	Register	Register
301 - 428	as above	as above	Data Input	Data Input	Register
501 - 528	as above	as above	Data Input	Register	Data Input
601 - 628	as above	as above	Data Input	Data Input	Data Input

Figure 15

International application No.
PCT/US 94/06157

A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 G11C7/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP,A,0 385 389 (NEC CORPORATION) 5 September 1990 see the whole document ---	1
A	EP,A,0 496 002 (FUJITSU) 29 July 1992 see the whole document ---	1
A	PATENT ABSTRACTS OF JAPAN vol. 12, no. 43 (P-664) 9 February 1988 & JP,A,62 191 971 (YAMAMOTO KAZUHIRO) see abstract ---	1
A	PATENT ABSTRACTS OF JAPAN vol. 12, no. 307 (P-747) 22 August 1988 & JP,A,63 076 195 (HITACHI) see abstract ---	1

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
18 October 1994	28.10.94.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 16, no. 252 (P-1367) 9 June 1992 & JP,A,04 060 586 (HITACHI) see abstract	1

1

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		US-A-	5148396	15-09-92
EP-A-0496002	29-07-92	JP-A-	4100150	02-04-92
		WO-A-	9203780	05-03-92

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